6MBP15XSD060-50

IGBT Modules

IGBT MODULE (X series)
600V / 15A / IPM

■ Features

Low-side IGBTs are separate emitter type
Short circuit protection
Temperature sensor output function
Under voltage protection
Fault signal output function
Input interface : TTL (3.3V/5V) Active high logic

■ Applications

AC 100 ~ 240V three phase inverter drive for small power
AC motor drives (such as compressor motor drive for
air conditioner, compressor motor drive for heat pump
applications, fan motor drive, ventilator motor drive)

■ Terminal assign and Internal circuit
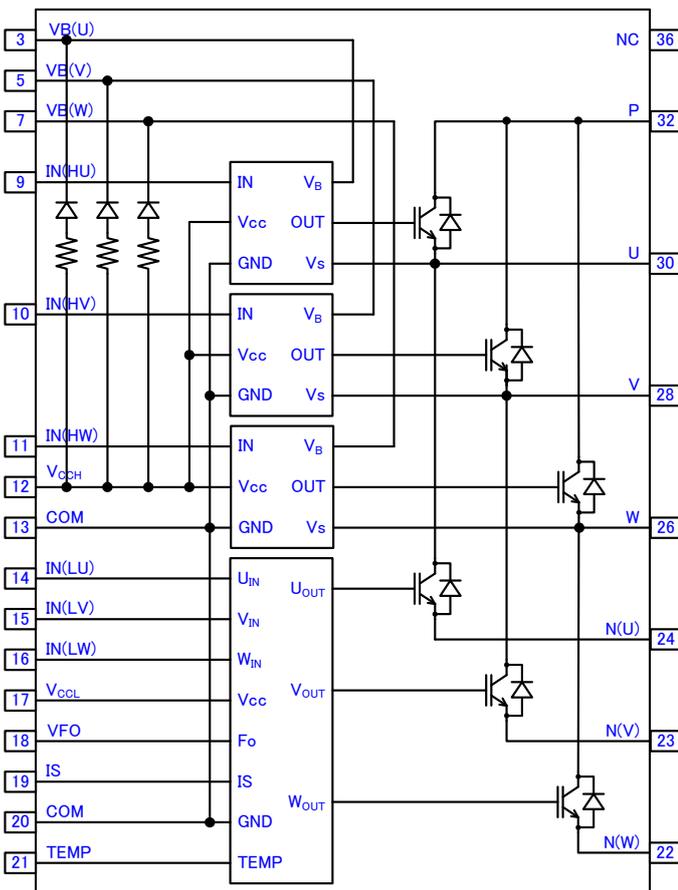
Pin No.	Pin Name	Pin Description
3	VB(U)	High-side bias voltage for U-phase IGBT driving
5	VB(V)	High-side bias voltage for V-phase IGBT driving
7	VB(W)	High-side bias voltage for W-phase IGBT driving
9	IN(HU)	Signal input for high side U-phase
10	IN(HV)	Signal input for high side V-phase
11	IN(HW)	Signal input for high side W-phase
12	V_{CCH}	High-side control supply
13	COM	Common supply ground
14	IN(LU)	Signal input for low side U-phase
15	IN(LV)	Signal input for low side V-phase
16	IN(LW)	Signal input for low side W-phase
17	V_{CCL}	Low-side control supply
18	VFO	Fault output
19	IS	Over current sensing voltage input
20	COM	Common supply ground
21	TEMP	Temperature sensor output
22	N(W)	Negative bus voltage input for W-phase
23	N(V)	Negative bus voltage input for V-phase
24	N(U)	Negative bus voltage input for U-phase
26	W	Motor W-phase output
28	V	Motor V-phase output
30	U	Motor U-phase output
32	P	Positive bus voltage input
36	NC	No Connection

■ Absolute Maximum Ratings at T$_j$=25°C, V$_{CC}$=15V (unless otherwise specified)

	Items	Symbol	Characteristics	Unit	Remarks
Inverter block	DC Bus Voltage	V$_{DC}$	450	V	Note *1
	Bus Voltage (Surge)	V$_{DC(Surge)}$	500	V	Note *1
	Collector-Emitter Voltage	V$_{CES}$	600	V	
	Collector Current	I$_{C@25}$	15	A	Note *2
	Peak Collector Current	I$_{CP@25}$	30	A	V$_{CC}$≧15V, V$_B$(*)≧15V Note *2, *3, *4
			20	A	V$_{CC}$≧13V, V$_B$(*)≧13V Note *2, *3, *4
	Diode Forward current	I$_{F@25}$	15	A	Note *2
	Peak Diode Forward current	I$_{FP@25}$	30	A	Note *2
	Collector Power Dissipation	P$_{D\_IGBT}$	32.5	W	per single IGBT T$_c$=25°C
	FWD Power Dissipation	P$_{D\_FWD}$	25.5	W	per single FWD T$_c$=25°C
	Junction Temperature	T$_j$	150	°C	
	Operating Junction Temperature	T$_{jOP}$	-40 ~ +150	°C	
Control circuit block	High-side Supply Voltage	V$_{CCH}$	-0.5 ~ 20	V	Applied between V$_{CCH}$-COM
	Low-side Supply Voltage	V$_{CCL}$	-0.5 ~ 20	V	Applied between V$_{CCL}$-COM
	High-side Bias Absolute Voltage	V$_{VB(U)-COM}$ V$_{VB(V)-COM}$ V$_{VB(W)-COM}$	-0.5 ~ 620	V	Applied between VB(U)-COM, VB(V)-COM, VB(W)-COM
	High-side Bias Voltage for IGBT gate driving	V$_{B(U)}$ V$_{B(V)}$ V$_{B(W)}$	-0.5 ~ 20	V	Note *4
	High-side Bias offset Voltage	V$_U$ V$_V$ V$_W$	-5 ~ 600	V	Applied between U-COM, V-COM, W-COM Note *5
	Input Signal Voltage	V$_{IN}$	-0.5 ~ V$_{CCH}$+0.5 / -0.5 ~ V$_{CCL}$+0.5	V	Note *6
	Input Signal Current	I$_{IN}$	3	mA	sink current
	Fault Signal Voltage	V$_{FO}$	-0.5 ~ V$_{CCL}$+0.5	V	Applied between V$_F$O-COM
	Fault Signal Current	I$_{FO}$	1	mA	sink current
	Over Current sensing Input Voltage	V$_{IS}$	-0.5 ~ V$_{CCL}$+0.5	V	Applied between IS-COM
	Junction Temperature	T$_j$	150	°C	
	Operating Case Temperature	T$_c$	-40 ~ +125	°C	See Fig.1-1
	Storage Temperature	T$_{stg}$	-40 ~ +125	°C	
	Isolation Voltage	V$_{iso}$	AC 1500	Vrms	Sine wave,60Hz t=1min , Note *7

Note *1 : Applied between P-N(U),P-N(V),P-N(W).
Note *2 : Pulse width and duty were limited by T$_j$max.
Note *3 : V$_{CC}$ is applied between V$_{CCH}$-COM,V$_{CCL}$-COM.
Note *4 : V$_B$(*) is applied between VB(U)-U,VB(V)-V, VB(W)-W.
Note *5 : Over 13.0V applied between VB(U)-U,VB(V)-V, VB(W)-W. This IPM module might make incorrect response if the high-side bias offset voltage is less than -5V.
Note *6 : Applied between IN(HU)-COM,IN(HV)-COM,IN(HW)-COM,IN(LU)-COM,IN(LV)-COM,IN(LW)-COM.
Note *7 : Applied between shorted all terminal and IMS (Insulated Metal Substrate).

■ Electrical Characteristics

● Inverter block (T_J=25°C unless otherwise specified)

Description	Symbol	Conditions		min.	typ.	max.	Unit
Zero gate Voltage Collector current	I_{CES}	V_{CE} = 600V V_{IN}= 0V	T_J=25°C	-	-	1	mA
			T_J=125°C	-	-	10	mA
Collector-Emitter saturation Voltage	$V_{CE(sat)}$	V_{CC}=+15V V_B(*)=+15V V_{IN}=5V Note *4	I_C=1.5A T_J=25°C	-	0.90	1.10	V
			I_C=15A T_J=25°C	-	1.60	1.90	
			I_C=15A T_J=125°C	-	1.75	2.10	
FWD Forward voltage drop	V_F	I_F=15A V_{IN}=0V	T_J=25°C	-	1.60	1.90	V
			T_J=125°C	-	1.50	-	
Turn-on time	t_{on}	V_{DC}=300V I_C=15A V_{CC}=15V V_B(*)=15V T_J=125°C V_{IN}=0V <-> 5V See Fig.2-1 Note *4		0.55	0.90	1.30	μs
Turn-on delay	$t_{d(on)}$				0.75	-	
Turn-on rise time	t_r			-	0.15	-	
VCE-IC Cross time of turn-on	$t_{c(on)}$			-	0.35	0.60	
Turn-off time	t_{off}			-	0.90	1.30	
Turn-off delay	$t_{d(off)}$			-	0.80	-	
Turn-off fall time	t_f			-	0.10	-	
VCE-IC Cross time of turn-on	$t_{c(off)}$			-	0.15	0.30	
FWD Reverse Recovery time	t_{rr}			-	0.20	-	

● **Control circuit block (T$_j$=25°C unless otherwise specified)**

Description	Symbol	Conditions		min.	typ.	max.	Unit
Circuit current of Low-side	I$_{CCL}$	V$_{CCL}$=15V	V$_{IN}$=5V	-	0.6	0.9	mA
		V$_{CCL}$=15V	V$_{IN}$=0V	-	0.6	0.9	
Circuit current of High-side	I$_{CCH}$	V$_{CCH}$=15V	V$_{IN}$=5V	-	1.25	1.9	mA
		V$_{CCH}$=15V	V$_{IN}$=0V	-	1.25	1.9	
Circuit current of Bootstrap circuit (per one uint)	I$_{CCHB}$	V$_B$(U)=15V, V$_B$(V)=15V, V$_B$(W)=15V	V$_{IN}$=5V	-	-	0.20	mA
			V$_{IN}$=0V	-	-	0.20	
Input Signal threshold voltage	Vth$_{(on)}$	Note *8 Pw≥0.9µs		-	2.1	2.6	V
	Vth$_{(off)}$			0.8	1.3	-	V
Input Signal threshold hysteresis voltage	Vth$_{(hys)}$			0.35	0.80	-	V
Operational input pulse width of turn-on	t$_{IN(ON)}$	V$_{IN}$=0V to 5V rise up, Note *6, Note *8		0.5	-	-	µs
Operational input pulse width of turn-off	t$_{IN(OFF)}$	V$_{IN}$=5V to 0V fall down Note *6, Note *8		0.7	-	-	µs
Input current	I$_{IN}$	V$_{IN}$=5V, Note *6		0.7	1.0	1.5	mA
Input pull-down resistance	R$_{IN}$	Note *6		3.3	5.0	7.2	kΩ
Fault Output Voltage	V$_{FO(H)}$	V$_{IS}$=0V, VFO terminal pull up to 5V by 10kΩ		4.9	-	-	V
	V$_{FO(L)}$	V$_{IS}$=1V, I$_{FO}$=1mA		-	-	0.95	V
Fault Output pulse width	t$_{FO}$	Note *9, See Fig.2-2, 2-3		20	-	-	µs

● **Control circuit block (continued)**

Description	Symbol	Conditions		min.	typ.	max.	Unit
Over Current Protection Voltage Level	V$_{IS(ref)}$	V$_{CC}$=15V Note *3, *10 See Fig.2-2		0.455	0.48	0.505	V
Over Current Protection Delay time	td$_{(IS)}$			0.3	0.8	1.3	µs
Output Voltage of temperature sensor	V$_{(temp)}$	Note *11	T$_C$=90°C	2.63	2.77	2.91	V
			T$_C$=25°C	0.88	1.13	1.39	V
Vcc Under Voltage Trip Level of Low-side	V$_{CCL(OFF)}$	T$_j$<150°C See Fig.2-3		10.3	-	12.5	V
Vcc Under Voltage Reset Level of Low-side	V$_{CCL(ON)}$			10.8	-	13.0	V
Vcc Under Voltage hysteresis	V$_{CCL(hys)}$			-	0.5	-	V
Vcc Under Voltage Trip Level of High-side	V$_{CCH(OFF)}$	T$_j$<150°C See Fig.2-4		8.3	-	10.3	V
Vcc Under Voltage Reset Level of High-side	V$_{CCH(ON)}$			8.8	-	10.8	V
Vcc Under Voltage hysteresis	V$_{CCH(hys)}$			-	0.5	-	V
VB Under Voltage Trip Level	V$_{B(OFF)}$	T$_j$<150°C See Fig.2-5		10.0	-	12.0	V
VB Under Voltage Reset Level	V$_{B(ON)}$			10.5	-	12.5	V
VB Under Voltage hysteresis	V$_{B(hys)}$			-	0.5	-	V
Forward voltage of Bootstrap diode	V$_{F(BSD)}$	T$_j$=25°C I$_{F(BSD)}$=10mA		0.90	1.4	1.90	V
	V$_{F(BSD)}$	T$_j$=25°C I$_{F(BSD)}$=100mA		2.3	4.3	6.3	

Note *8 : This IPM module might make incorrect response if the input signal pulse width is less than t$_{IN(on)}$ and t$_{IN(off)}$.
Note *9: Fault signal is asserted corresponding to an "Over-current protection", an "Under-voltage protection" at low-side, and an "Over-heat protection".
     Under the condition of "Over-current protection" or "Under-voltage protection" or "Over-heat protection", the fault signal is asserted continuously while these conditions are continuing. However, the minimum fault output pulse width is minimum 20µsec even if very short failure condition (which is less than 20µs) is triggered.
Note *10 : Over current protection is functioning only for the low-side arms.
Note *11 : Fig.1-1 shows the measurement position of temperature sensor.

■ Thermal Characteristics

Description	Symbol	min.	typ.	max.	Unit
Junction to Case Thermal Resistance (per single IGBT) Note *12	$R_{th(j-c)\_IGBT}$	-	-	3.85	°C/W
Junction to Case Thermal Resistance (per single FWD) Note *12	$R_{th(j-c)\_FWD}$	-	-	4.95	°C/W

Note *12: Thermal compound with good thermal conductivity should be applied evenly with about +100μm~+200μm on the contacting surface of this device and heat-sink.

■ Mechanical Characteristics

Description	Symbol	Conditions	min.	typ.	max.	Unit
Tighten torque	-	Mounting screw: M3	0.59	0.69	0.98	Nm
Heat-sink side flatness	-	Note. *13	0	-	100	μm
Weight	-	-	-	9.3	-	g

Note *13: Fig.1-2 shows the measurement position of heat sink flatness

■ Recommended Operation Conditions

● All voltages are absolute voltages referenced to Vcc –potential unless otherwise specified.

Description	Conditions	min.	typ.	max.	Unit
DC Bus Voltage	V_{DC}	0	300	400	V
High-side Bias Voltage for IGBT gate driving	$V_B(*)$	13.0	15.0	18.5	V
High-side Supply Voltage	V_{CCH}	13.5	15.0	16.5	V
Low-side Supply Voltage	V_{CCL}	13.5	15.0	16.5	V
Control Supply variation	ΔV_B	-1	-	1	V/μs
	ΔV_{CC}	-1	-	1	
Input signal voltage	V_{IN}	0	-	5	V
Voltage for current sensing	V_{ISC}	0	-	5	V
Potential difference of between COM to N (including surge)	V_{COM_N}	-5	-	5	V
Dead time for preventing arm-short (Tc≤125°C)	t_{DEAD}	1.0	-	-	μs
Allowable output current (Note *14)	I_O	-	-	15.0	A rms
Allowable minimum input pulse width (Note *15, Note *16)	$PW_{IN(on)}$	0.5	-	-	μs
	$PW_{IN(off)}$	0.7	-	-	μs
PWM Input frequency	f_{PWM}	-	-	20	kHz
Operating Junction Temperature	$T_{j(ope)}$	-30	-	150	°C

Note *14: V_{DC}=300V, V_{CCH}=Vcc$L$=V$_B$(*)=15V, PF=0.8, Sinusoidal PWM, 3phase modulation, Tj≤150°C ,Tc≤100°C , f$_{PWM}$=5kHz, fo=200Hz, Ks=0.9
Note *15: In the pulse width of 0.5us, the loss of IGBT increases for the saturation operation.
          To reduce the loss of IGBT, please enlarge the pulse width more than the switching time of IGBT.
Note *16: This IPM module might response according to input signal pulse even when the input signal pulse width is less than $PW_{IN(on)}$ and $PW_{IN(off)}$.
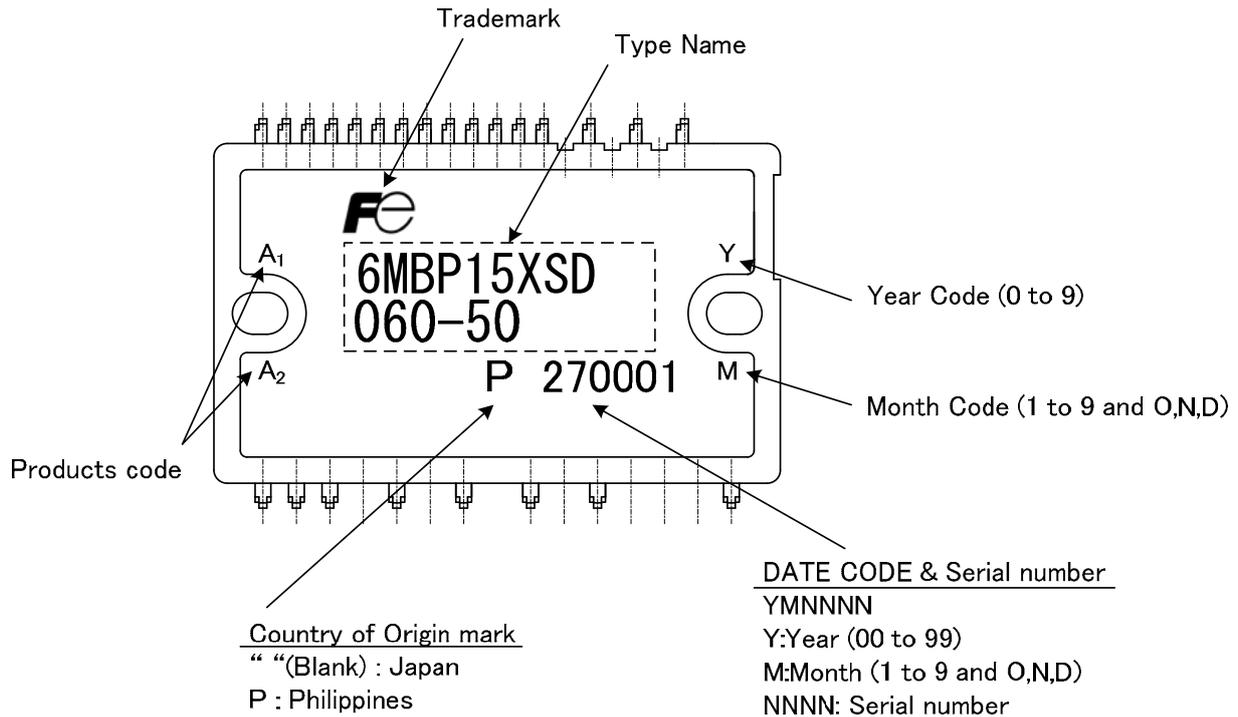
■ Package outline dimensions

C

A

43.0±0.5
18x1.778(=32.004)
35.0±0.3
1.778±0.2
26.0±0.5
13.0
3.2±0.1
10.6±0.1
2.6±0.1
1.6±0.1
4.2±0.1
0.98(min.)
2.54±0.2
3.50(min.)
8.58(min.)
14x2.54 (=35.56)

B

0.40±0.1
1.8±0.1
29.4±0.5
14.7±0.5
14.0±0.5
0.40±0.1
1.8±0.1
1.5±0.1
3.7±0.1

Insulated Metal Substrate

Solder Plating

14.13±0.5
5.63±0.5
3.83±0.25
0.13±0.13 ※Note.1

D

Insulated Metal Substrate

30.4±0.3
13.0±0.3
8.96±0.3
4.76±0.3
0.7±0.4
15.56±0.3
15.56±0.3

DETAIL A
2.5(min)
(0.6)
(1.2)

DETAIL B
3.50(min.)

DETAIL C
2.5(min)
0.6±0.1
0.9±0.1

DETAIL D
1.2±0.1
0.6±0.1
3.50(min.)

Unit: mm

Note ※1: The IMS(Insulated Metal Substrate) deliberately protruded from back surface of case.
It is improved of thermal conductivity between IMS and heat-sink.

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
3	VB(U)	14	IN(LU)	22	N(W)
5	VB(V)	15	IN(LV)	23	N(V)
7	VB(W)	16	IN(LW)	24	N(U)
9	IN(HU)	17	V_{CCL}	26	W
10	IN(HV)	18	VFO	28	V
11	IN(HW)	19	IS	30	U
12	V_{CCH}	20	COM	32	P
13	COM	21	TEMP	36	NC

■ Marking

Trademark

Type Name

6MBP15XSD
060-50

P 270001

A₁

A₂

Y

M

Year Code (0 to 9)

Month Code (1 to 9 and O,N,D)

Products code

Country of Origin mark
" "(Blank) : Japan
P : Philippines

DATE CODE & Serial number
YMNNNN
Y:Year (00 to 99)
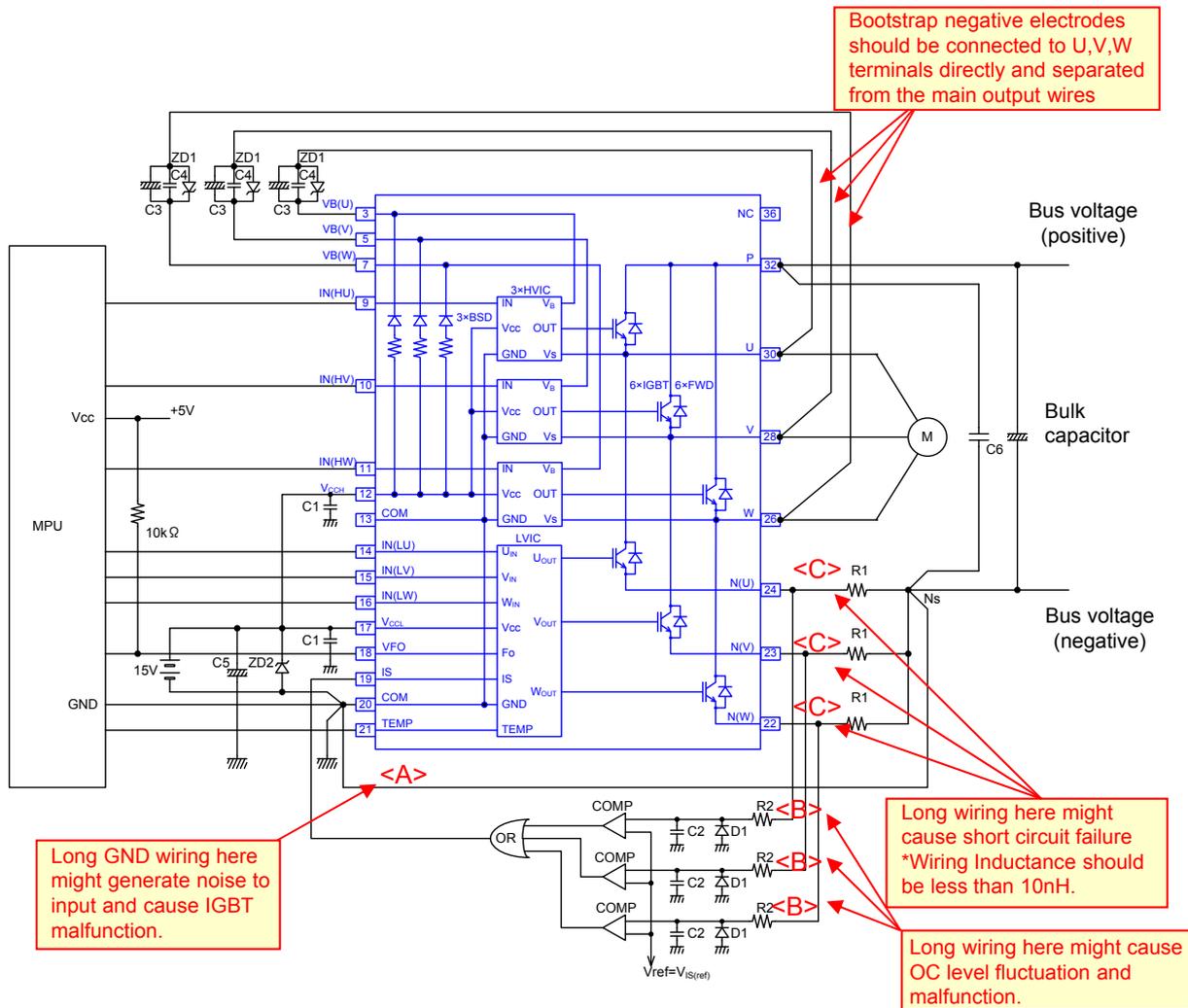M:Month (1 to 9 and O,N,D)
NNNN: Serial number

Note : Product code A₁ means current ratings , and "L" is marked.
        Product code A₂ means variations , and "D" is marked.

■ An example of application circuit.

● Fig. shows an example of an application circuit.

Bootstrap negative electrodes should be connected to U,V,W terminals directly and separated from the main output wires

Long GND wiring here might generate noise to input and cause IGBT malfunction.

Long wiring here might cause short circuit failure *Wiring Inductance should be less than 10nH.

Long wiring here might cause OC level fluctuation and malfunction.

Note *1: Input signal for drive is High-Active. There is a pull-down resistor built in the IC input circuit. To prevent malfunction, the wiring of each input should be as short as possible. When using R-C coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.

Note *2: By the function of the HVIC, it is possible of the direct coupling to microprocessor (MPU) without any photo-coupler or pulse-transformer isolation.

Note *3: VFO output is open drain type. It should be pulled up to the positive side of a 5V power supply by a resistor of about 10kΩ.

Note *4: To prevent erroneous protection, the wiring of (A), (B), (C) should be as short as possible.

Note *5: The time constant R2-C2 of the protection circuit should be selected approximately 1.5μs.
　　　　 Over current (OC) shutdown time might vary due to the wiring pattern. Tight tolerance, temp-compensated type is recommended for R2, C2.

Note *6: Please set the threshold voltage of the comparator reference input to be same as the IPM OC trip reference voltage $V_{IS(ref)}$.

Note *7: Please use high speed type comparator and logic IC to detect OC condition quickly.

Note *8: If negative voltage of R1 at the switching timing is applied, the schottky barrier diode D1 is recommended to be inserted parallel to R1.

Note *9: All capacitors should be mounted as close to the terminals of the IPM as possible. (C1, C4 : narrow temperature drift, higher frequency and DC bias characteristic ceramic type are recommended, and C3, C5: narrow temperature drift, higher frequency and electrolytic type.)

Note *10: To prevent surge destruction, the wiring between the snubber capacitor and the P terminal ,Ns node should be as short as possible. Generally a 0.1μ to 0.22μF snubber capacitor (C6) between the P terminal and Ns node is recommended.

Note *11: Two COM terminals (13 & 20 pin) are connected inside the IPM, it must be connected either one to the signal GND outside and leave another one open.

Note *12: It is recommended to insert a zener-diode (22V) between each pair of control supply terminals to prevent surge destruction.

Note *13: If signal GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect signal GND and power GND at only a point.

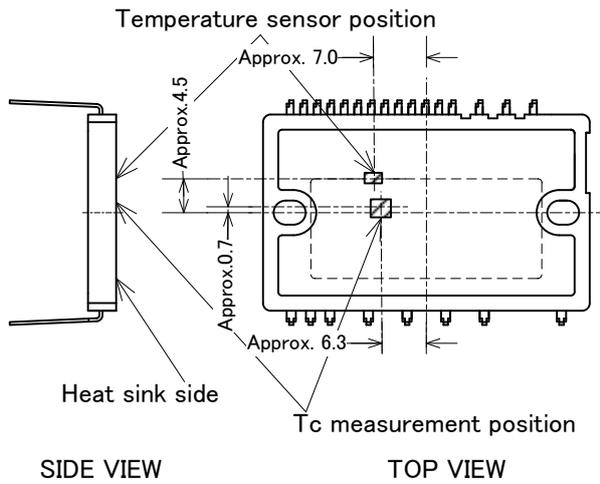Fig.1-1: The measurement position of temperature sensor.

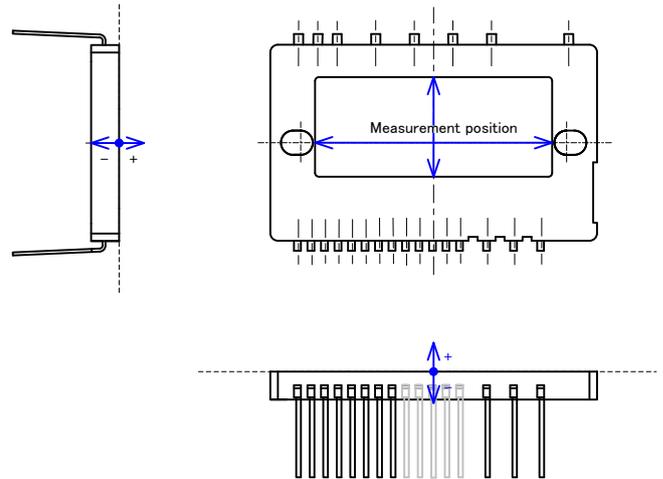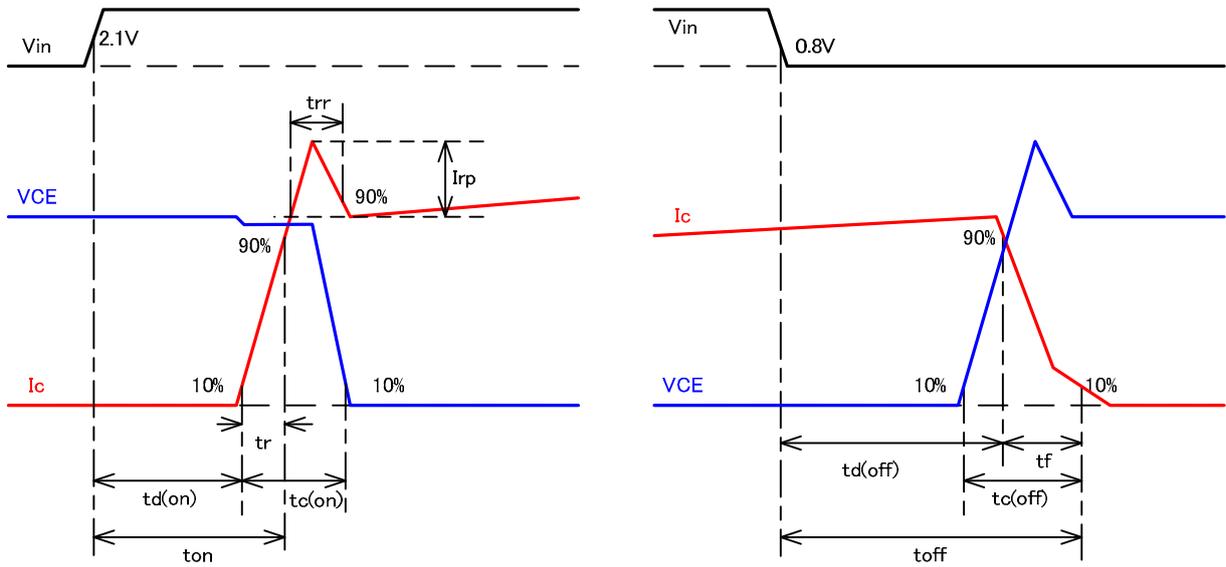Fig.1-2: The measurement position of heat sink flatness

Temperature sensor position

Approx. 7.0

Approx.4.5

Approx.0.7

Approx. 6.3

Heat sink side

Tc measurement position

SIDE VIEW   TOP VIEW

Measurement position

Fig.2-1: Switching waveforms

Vin   2.1V

trr

Irp

VCE

90%

90%

Ic   10%   10%

tr

td(on)   tc(on)

ton

Vin   0.8V

Ic

90%

VCE   10%   10%

td(off)   tf

tc(off)

toff

Fig.2-2: Operation sequence of Over current protection

Operation sequence of Over Current protection
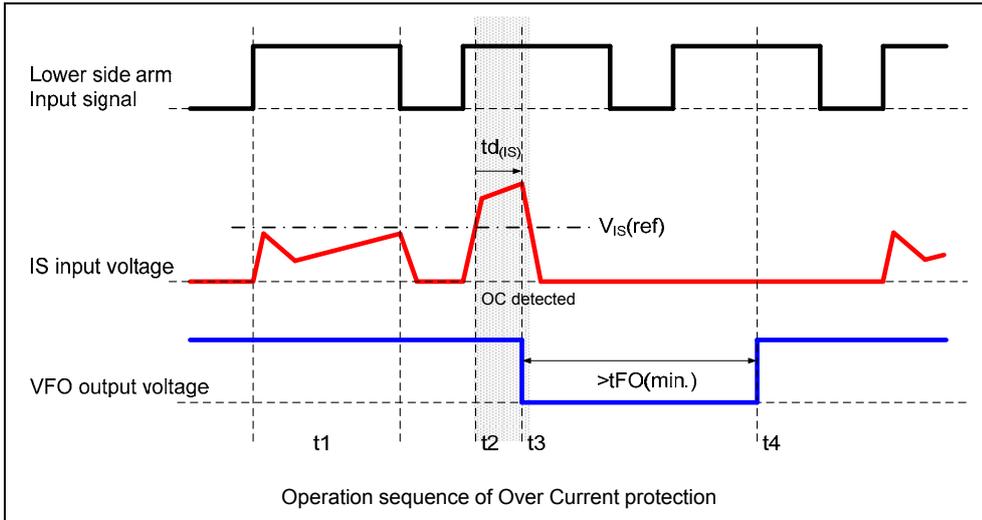
t1: IS input voltage does not exceed V_{IS}(ref), while the collector current of the lower side IGBT is under the normal operation.

t2: When IS input voltage exceeds V_{IS}(ref), the OC is detected.

t3: The fault output VFO is activated and all lower side IGBT shut down simultaneously after the over current protection delay time $td_{(IS)}$. Inherently there is dead time of LVIC in $td_{(IS)}$.

t4: After the fault output pulse width tFO, the OC is reset. Then next input signal is activated.

Fig.2-3: Operation sequence of V_{CCL} Under voltage trip (lower side arm)

Operation sequence of V_{CCL} Under Voltage protection (lower side arm)
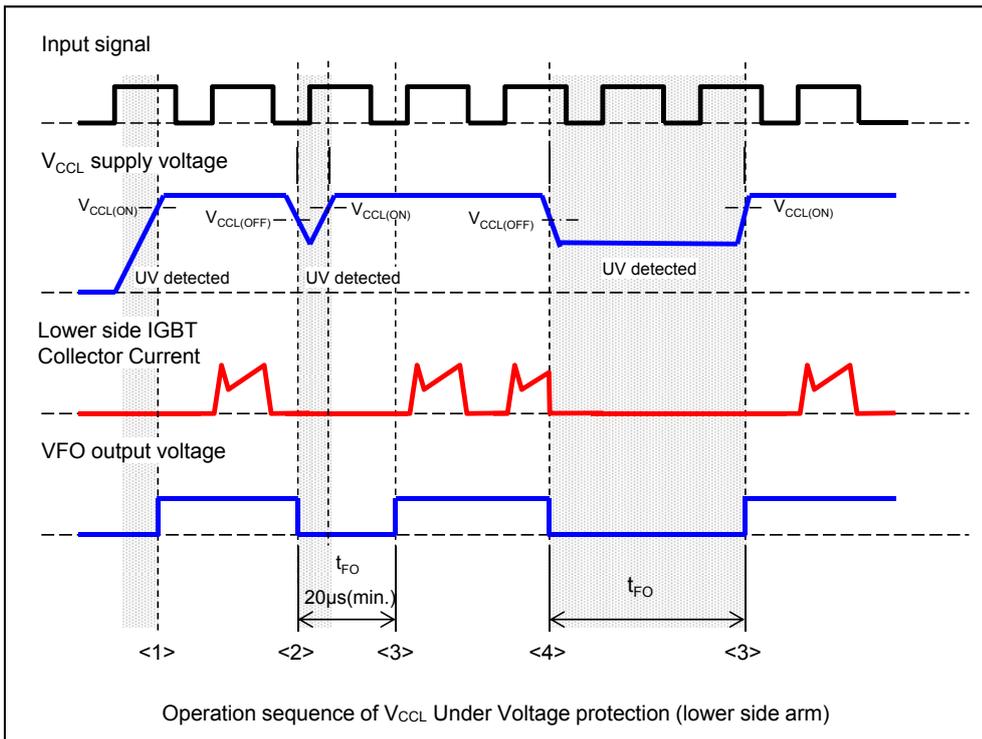
When V_{CCL} is under 4V, UV and fault output are not activated.

<1> When V_{CCL} is under $V_{CCL(ON)}$, all lower side IGBTs are OFF state.
After V_{CCL} rises $V_{CCL(ON)}$, the fault output VFO is released (high level).
And the LVIC starts to operate, then next input is activated.

<2> The fault output VFO is activated when V_{CCL} falls below $V_{CCL(OFF)}$, and all lower side IGBT remains OFF state.
When the voltage drop time is less than 20μs, the fault output pulse width is generated minimum 20μs and all lower side IGBTs are OFF state in spite of input signal condition during that time.

<3> UV is reset after t_{FO} when V_{CCL} exceeds $V_{CCL(ON)}$ and the fault output VFO is reset simultaneously.
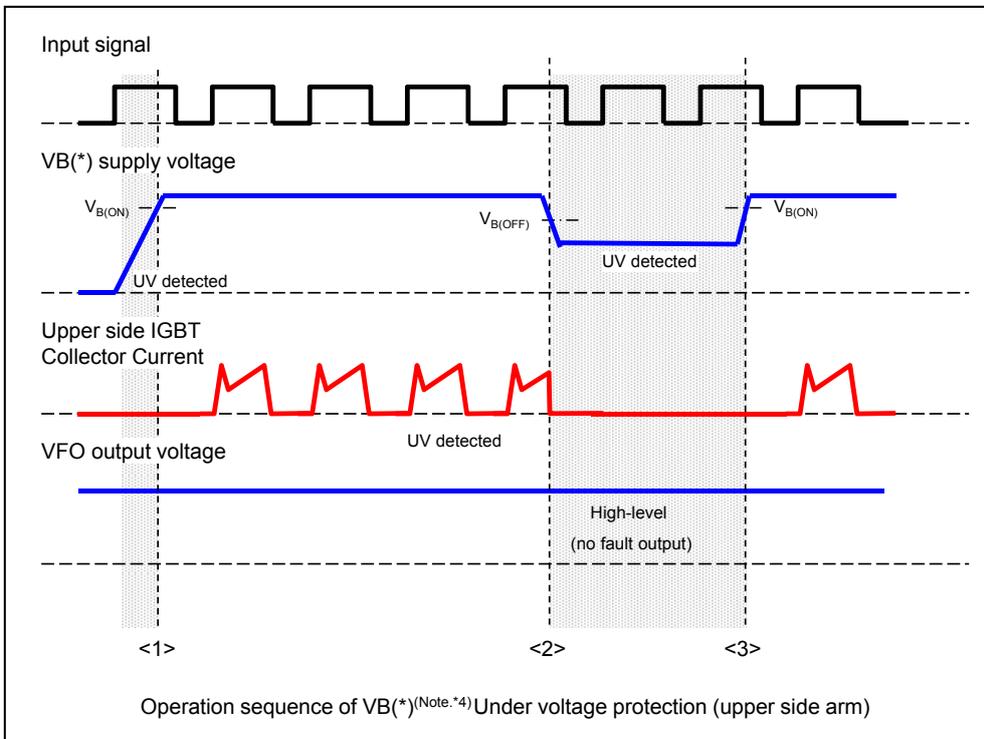And the LVIC starts to operate, then next input is activated.

<4> When the voltage drop time is more than t_{FO}, the fault output pulse width is generated and all lower side IGBTs are OFF state in spite of input signal condition during the same time.

Fig.2-4: Operation sequence of V_{CCH} Under voltage trip (upper side arm)

Operation sequence of V_{CCH} Under Voltage protection (upper side arm)
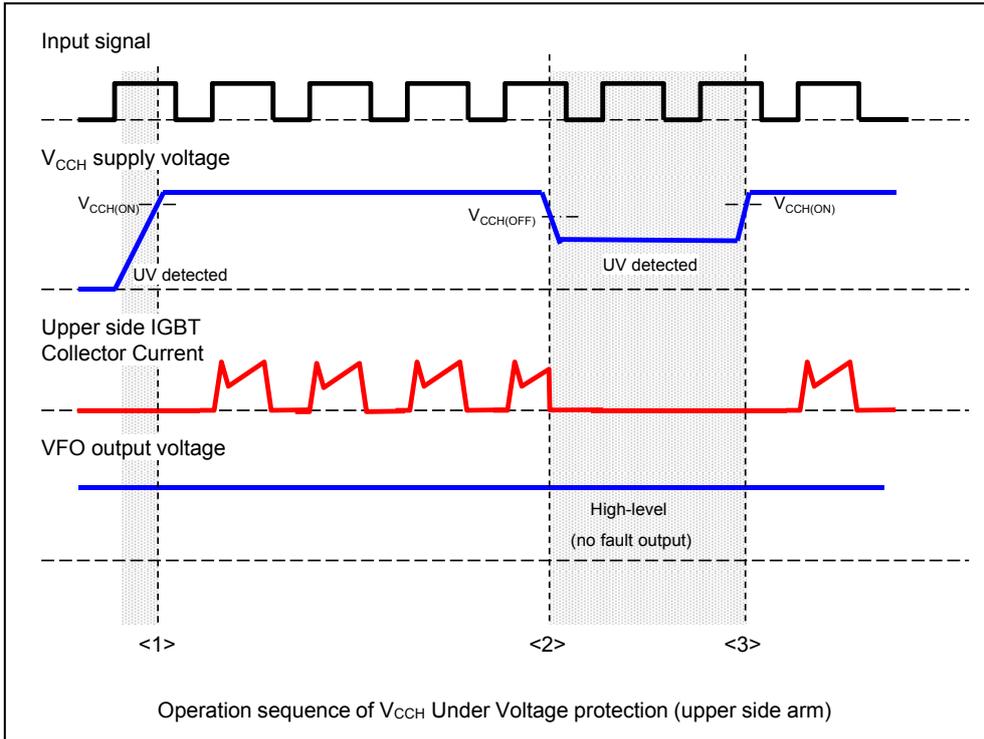
<1> When V_{CCH} is under $V_{CCH(ON)}$, the upper side IGBT is OFF state.
After V_{CCH} exceeds $V_{CCH(ON)}$, the HVIC starts to operate. Then next input is activated.
The fault output VFO is constant (high level) not to depend on V_{CCH}.
<2> After V_{CCH} falls below $V_{CCH(OFF)}$, the upper side IGBT remains OFF state.
But the fault output VFO keeps high level.
<3> The HVIC starts to operate after UV is reset, then next input is activated.

Fig.2-5: Operation sequence of VB Under voltage trip (upper side arm)

Operation sequence of VB(*)(Note.*4) Under voltage protection (upper side arm)

<1> When VB(*) is under $V_{B(ON)}$, the upper side IGBT is OFF state.
After VB(*) exceeds $V_{B(ON)}$, the HVIC starts to operate. Then next input is activated.
The fault output VFO is constant (high level) not to depend on VB(*). (Note*14)
<2> After VB(*) falls below $V_{B(OFF)}$, the upper side IGBT remains OFF state.
But the fault output VFO keeps high level.
<3> The HVIC starts to operate after UV is reset, then next input is activated.

Note *14: The fault output is not given HVIC bias conditions.

WARNING

1. This Catalog contains the product specifications, characteristics, data, materials, and structures as of March 2016.
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